CS315-02 Processor Design Components

C Coding

Data representation

Memory

RISC-V Assembly

RISC-V Machine Code

RISC-V Emulator

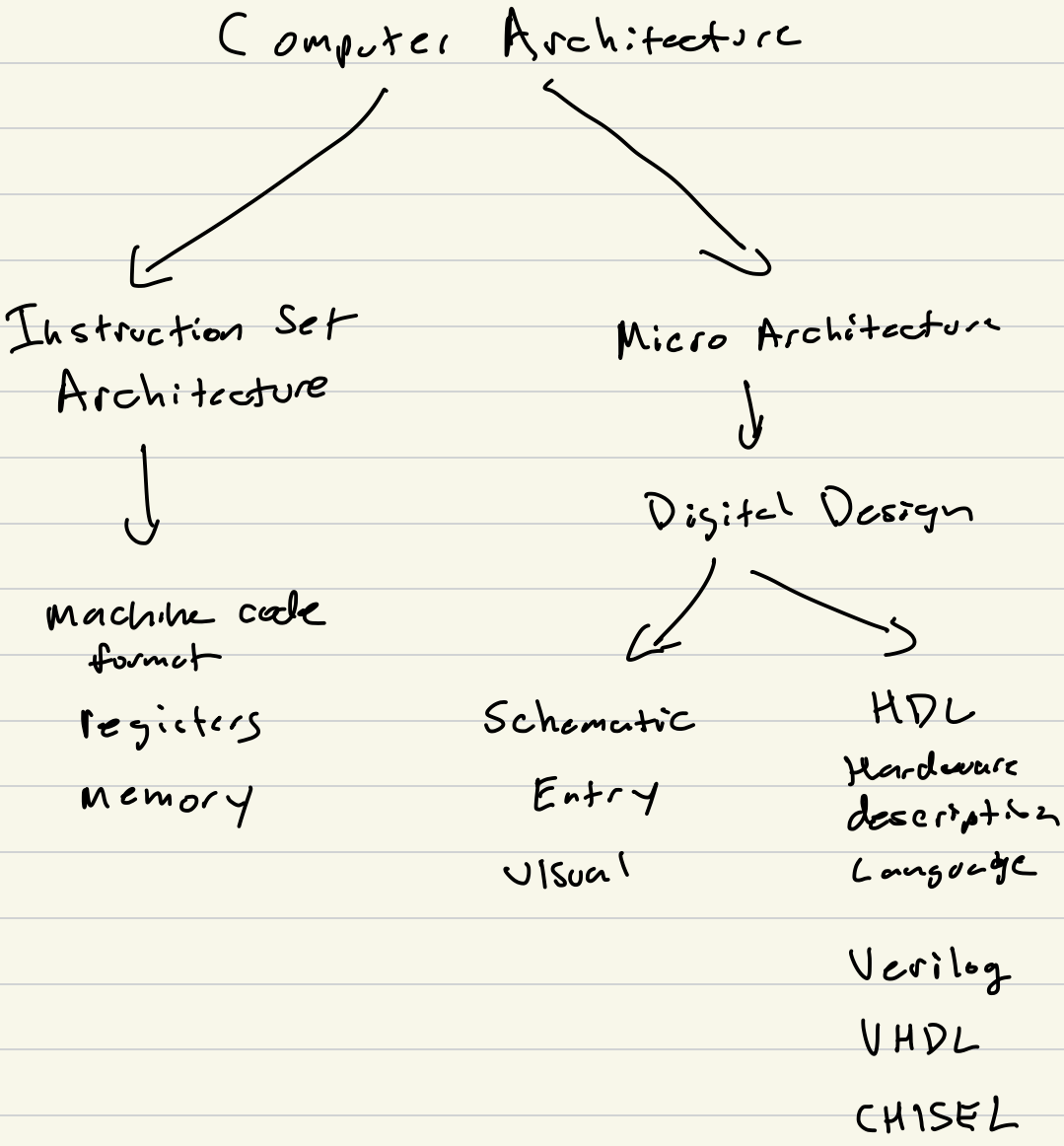
Cache Design

Digital Design

Processor Design

Instruction Set Architecture (ISA)

Micro Architecture ← implemented in digital logic


Computer Architecture
Instruction Set Architecture
machine code format
registers
memory
Micro Architecture
Digital Design
Schematic Entry
Visual
HDL
Hardware description Language
Verilog
VHDL
CHISEL

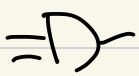
Processor Design

Moore's Law

The number of transistors doubles every 1.5 years

↑

increase size
increase density



↑ 2-3 transistor

Two micro architectures

Single-Cycle Processor

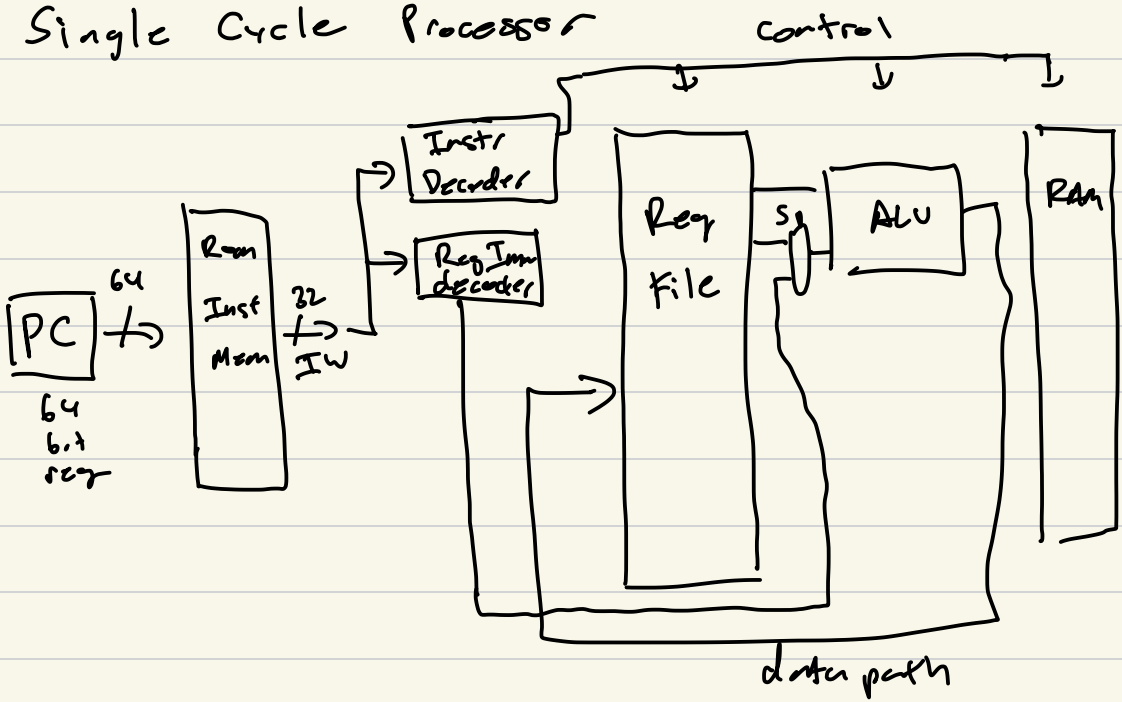
Pipelined Processor

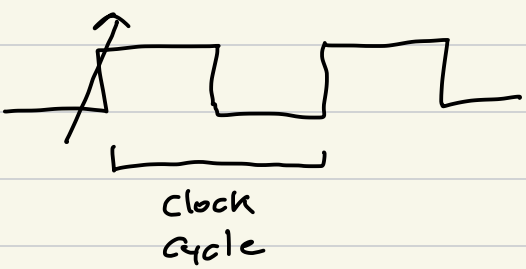
Superscalar
Out of order execution
Speculative execution

Lab05 → Lab 06 → Project06

add t0, a0, a1 addi t0, t1, 99

Single Cycle Processor





Register File

32 64-bit Registers: $x0, x1, \ldots, x31$

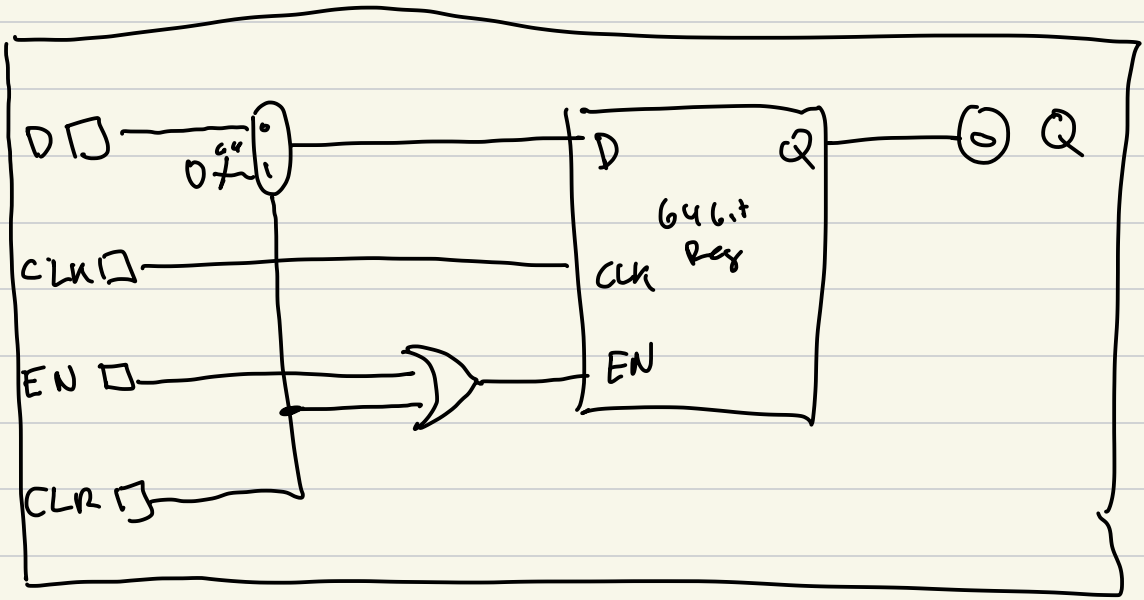
Read upto two register values in a single clock cycle and write to one register. x0 (zero) will always be 0, cannot be updated.

RR - read reg #
RD - read data

WR - write register
WD - write data
WE - write enable

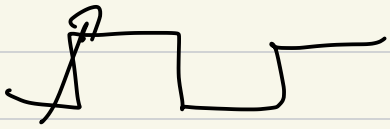
add t0, t1, t2

Adding CLR to Digital Register

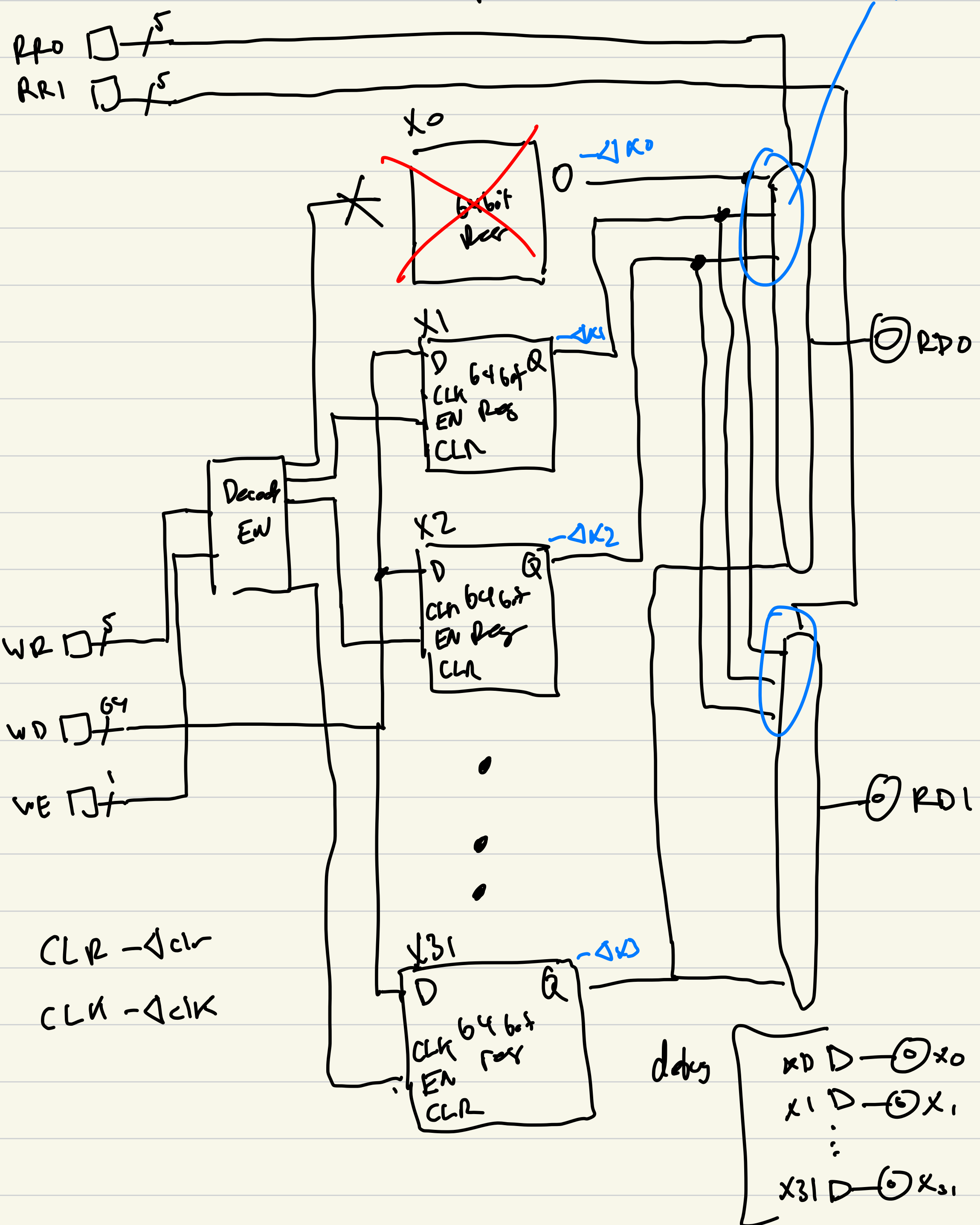


64 bit Reg CLR

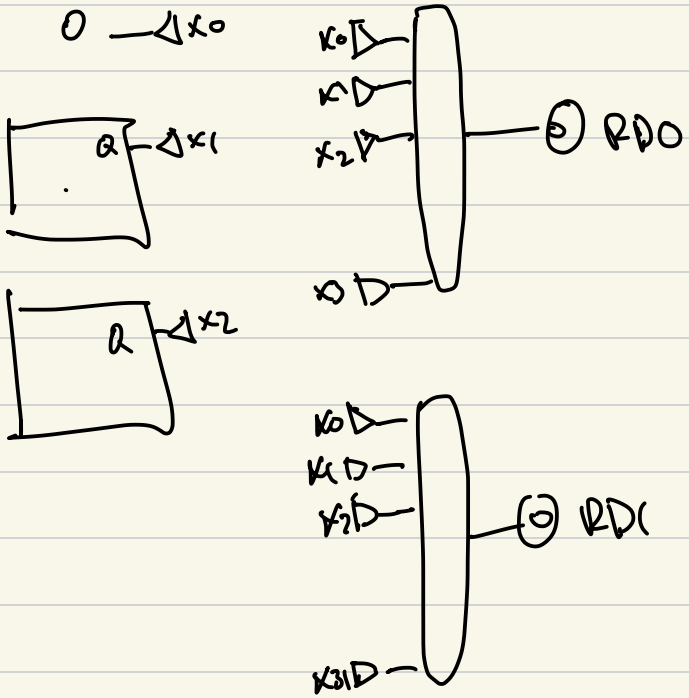
Synchronous clear



Register File Implementation



Tunnels



add t0, t1, t1

Decoder with EN

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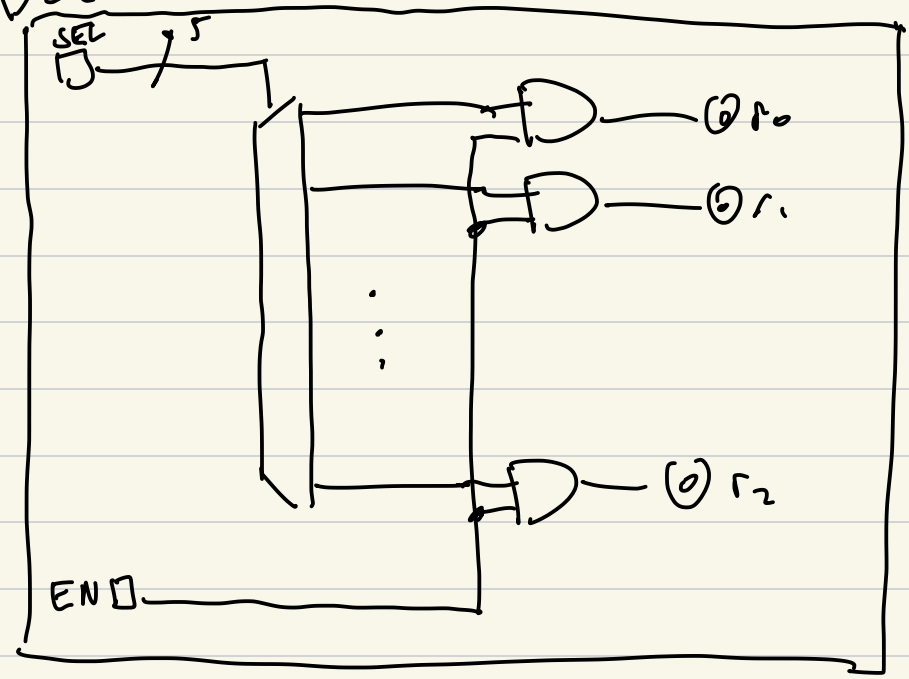

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